



<b>LIST OF REFERENCES CITED BY APPLICANT</b> <i>(Use several sheets if necessary)</i>				ATTY. DOCKET NO.: <b>4717-7300</b>		APPLICATION NO.: <b>10/763,978</b>	
				APPLICANT: <b>Cecile AULNETTE et al.</b>			
				FILING DATE: <b>January 22, 2004</b>		GROUP: <b>2811</b>	
<b>U.S. PATENT DOCUMENTS</b>							
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
Phe	AA	6,039,803	3/2000	Fitzgerald et al.	117	89	
	AB	2002/0084000 A1	7/2002	Fitzgerald	148	33.2	
	AC						
<b>FOREIGN PATENT DOCUMENTS</b>							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	AD						
	AE						
<b>OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
✓ AF	B. Gallas et al., "Influence of misfit and threading dislocations on the surface morphology of SiGe graded-layers"; Journal of Crystal Growth 201/202, pp 547-550, (1999)						
✓ AG	Douglas Paul, "The Physics, Material and Devices of Silicon Germanium Technology", Physics World, pp. 1-14.						
✓ AH	Asano et al., "Structural characterization of Si <sub>1-x</sub> Ge <sub>x</sub> alloy layers grown by molecular beam epitaxy on Si(001) substrates", American Institute of Physics, Journal of Applied Physics, Vol. 87, No. 12, pp 8759-8765 (2000)						
AI							
AJ							
<b>EXAMINER</b>  				<b>DATE CONSIDERED</b>  23 Jun 05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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<i>See</i>	AA	5,770,868	6/1998	Gill et al.	257	190	
	AB	6,059,895	5/2000	Chu et al.	148	33.1	
	AC	2002/0017642	2/2002	Mizushima et al.	257	19	


  

FOREIGN PATENT DOCUMENTS								
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	✓AD	EP 1 253 648	10/2002	European Patent Office	H01L	29/78	X	
	✓AE	WO 02 15244	2/2002	PCT	H01L	21/205	X	

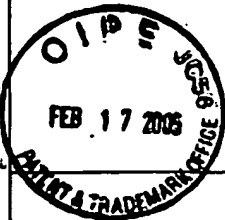


  

OTHER REFERENCES <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>	
✓AF	Cheng et al., "SiGe-on-Insulator (SGOI): Substrate Preparation and MOSFET Fabrication for Electron Mobility Evaluation," IEEE International SOI Conference, 10/01, pp. 13-14 (2001).
✓AG	Colinge, "Silicon-on-Insulator Technology," VLSI, p. 47.
✓AH	Huang et al., "Electron and Hole Mobility Enhancement in Strained SOI by Wafer Bonding," <i>IEEE Transactions on Electron Devices</i> , vol. 49, no. 9, pp. 1566-71 (Sep. 2002).
✓AI	Iyer & Auberton-Herve (ed.), "Silicon Wafer Bonding Technology," EMIS Processing Series No. 1, pp. 22, 36, 57.
✓AJ	Li et al., "Investigation of strain relaxation of Ge <sub>1-x</sub> Si <sub>x</sub> epilayers on Ge(001) by high-resolution x-ray reciprocal space mapping," <i>Semiconductor Science and Technology</i> , vol. 10, pp. 1621-28 (Dec. 1995).
✓AK	Takagi et al., "Device structure and electrical characteristics of strained-Si-on-insulator (strained-SOI) MOSFETs," <i>Material Science and Engineering</i> , vol. 89, no. 1-3, pp. 426-434 (Feb. 2002).
✓AL	Taraschi et al., "Relaxed SiGe-on-insulator fabricated via wafer bonding and etch back," <i>J. Vac. Sci. Technol.</i> , B 20(2), pp. 725-27 (Mar/Apr. 2002).
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AD	TW512487 English Abstract	12/2002	Taiwanese			X	
AE							
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